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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,923	06/07/2004	Min-Lung Huang	10788-US-PA	3922

31561 7590 05/30/2008

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
05/30/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/709,923	HUANG ET AL.	
	Examiner	Art Unit	
	Alonzo Chambliss	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 16* is/are allowed.

6)☒ Claim(s) *6-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/5/08 has been entered.

Response to Arguments

2. Applicant's arguments filed 5/5/08 have been fully considered but they are not persuasive. In regards to the bump structure not taught by Degani. However, Sakuyama discloses a bump structure on a substrate as seen in Fig. 3A.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were

made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 6-8, 10, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. (US 6,534,723) in view of Sakuyama et al. (US 6,689,639) and Degani et al. (US 5,564,617).

With respect to Claims 6 and 14, Asai discloses providing a substrate (i.e. the combination of 34, 46, 50, 52, and 54 or 46, 70, 72, 74,and 76) having a first surface and an opposite second surface, wherein the substrate includes a plurality of first contacts 40 on the first surface of the substrate and wherein the first contacts are electrically connected to the second contacts 40. A plurality of bumps 62 on the first surface of the substrate, wherein each bump 62 is connected to one first contact 10. A chip 82 has a plurality of bonding pads corresponding to the bumps 62. Arranging the chip 82 onto the first surface of the substrate by flipping the chip 82, so that the bonding pads are connected to the bumps 10 and reflowing the bumps 62 (see col. 2 lines 42-59, col. 18 lines 12-67, and col. 19 lines 1-45; Figs. 7-10). Asai fails to disclose a metal layer made of Ni disposed on surfaces of the bonding pads of a chip. A plurality of bumps connected to one first contact and has a smooth curving top surface. However, Sakuyama discloses a metal layer 20 (i.e. the combination of layers 21-23) is made of Ni disposed on surfaces of the bonding pads 11 of a chip 10. A plurality of bumps

connected to one first contact 41 and has a smooth curving top surface (see col. 6 lines 46-53; Figs. 1D, 2A-2D, 3A-3C, 4A, 4B, 5, 6D, and 7A-7C). It is well known in the semiconductor industry to have a chip without having an additional bumps thereon as evident by Degani (see Figs. 2-4). Thus, Asai and Sakuyama have substantially the same environment of a chip electrically connected to a substrate by solder bumps. Therefore, one skilled in the art at the time of the invention would readily recognize incorporating a metal layer on the surface of the bonding pads of Asai, since the metal layer would improve the electrical connection between the solder bumps and the bonding pads as taught by Sakuyama.

With respect to Claims 7 and 8, Asai discloses disposing a plurality of solder balls or pins 64 or 66 on the second surface of the substrate, wherein the solder balls or pins are connected to the second contacts (see Figs.7, 8, and 10).

With respect to Claim 10, Sakuyama discloses forming the bumps comprises printing a tin paste onto surfaces of the first contacts and reflowing the tin paste (see col. 2 lines 4-30 and col. 7 lines 38-45).

With respect to Claim 13, Sakuyama discloses filling an underfill material 72 between the chip and the substrate, wherein the underfill material covers the bumps (see Fig. 5).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. (US 6,534,723), Sakuyama et al. (US 6,689,639), and Degani et al. (US 5,564,617) as applied to claim 1 above, and further in view of Acocella et al. (US 5,591,941).

With respect to Claim 9, Asai-Sakuyama-Degani discloses the claimed invention except for forming the bumps comprising implanting tin globes and treating surfaces of the first contacts with a flux before implanting tin globes (see col. 5 lines 20-59; Fig. 5). Thus, Asai-Sakuyama-Degani and Acocella have substantially the same environment of bumps formed on a substrate. Therefore, one skilled in the art at the time of the invention would readily recognize incorporating a flux on the first contact pad of Asai-Sakuyama-Degani, since the flux would facilitate connection between the bump and the contact pad as taught by Acocella.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. (US 6,534,723), Sakuyama et al. (US 6,689,639), and Degani et al. (US 5,564,617) as applied to claim 1 above, and further in view of Gansauge et al. (US 5,244,833).

With respect to Claim 11, Asai-Sakuyama discloses the claimed invention except for forming the bumps on surface of the first contacts by electroplating, thus forming the bumps on the substrate without reflowing. However, Gansauge discloses forming the bumps on surface of the first contacts by electroplating, thus forming the bumps on the substrate without reflowing (see col. 4 lines 7-13 and col. 5 lines 40-45). Thus, Asai-Sakuyama-Degani and Gansauge have substantially the same environment of bumps formed on a substrate. Therefore, one skilled in the art at the time of the invention would readily recognize substitute a electroplating process for process used by Asai-Sakuyama-Degani to form the bumps, since the electroplating process would facilitate connection between the bump and the contact pad as taught by Gansauge.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. (US 6,534,723), Sakuyama et al. (US 6,689,639), and Degani et al. (US 5,564,617) as applied to claim 1 above, and further in view of Benenati et al. (US 6,177,729).

With respect to Claim 12, Asai-Sakuyama-Degani discloses the claimed invention except for an adhesive layer formed on the surfaces of the bonding pads of the chip before the chip is arranged to the substrate, and wherein after the chip is arranged to the substrate, the adhesive layer wraps around the bumps. However, Benenati discloses an adhesive layer 22 or 38 formed on the surfaces of the bonding pads 24 of the chip 26 before the chip 26 is arranged to the substrate 28, and wherein after the chip 26 is arranged to the substrate 28, the adhesive layer 22 or 38 wraps around the bumps 20 (see col. 4 lines 1-67 and col. 5 lines 1-14; Figs. 1, 3a-3c, 5a, 5c, 6a, 6b, and 8). Thus, Asai-Sakuyama-Degani and Benenati have substantially the same environment of a chip attached to a substrate by bumps. Therefore, one skilled in the art at the time of the invention would readily recognize incorporating an adhesive to the contact of the chip of Asai-Sakuyama-Degani, since the adhesive would facilitate connection between the bump and the contact pad of the chip as taught by Benenati.

Allowable Subject Matter

8. Claims 15 and 16 are allowable over the prior art.

9. The following is a statement of reason for the indication of allowance subject matter: the prior art of record does not teach or suggest the combination of forming a

conductive adhesive layer on the metal layer, wherein the conductive adhesive layer has a second melting point lower than the first melting point of the bumps. A

arranging the chip onto the first surface of the substrate by flipping the chip, so that the bonding pads with the adhesive layer are connected to the bumps. Reflowing the conductive adhesive layer for wrapping the bumps wherein the bumps remain not melted in claim 15.

The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

Conclusion

10. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you

have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.

AC/May 25, 2008

/Alonzo Chambliss/
Primary Examiner, Art Unit 2892